

FIG. 1
 (PRIOR ART)

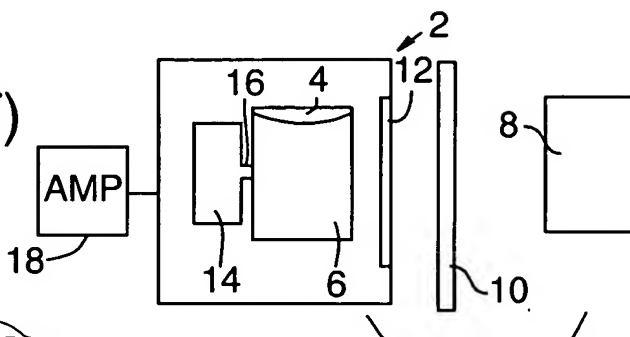


FIG. 2
 (PRIOR ART)

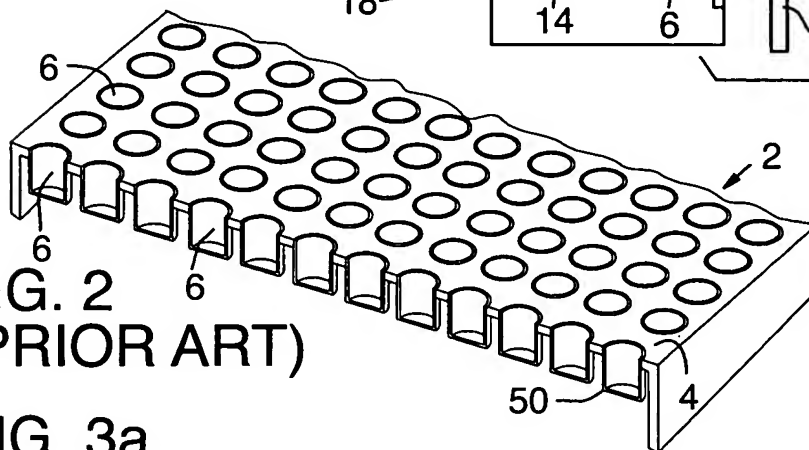


FIG. 3a

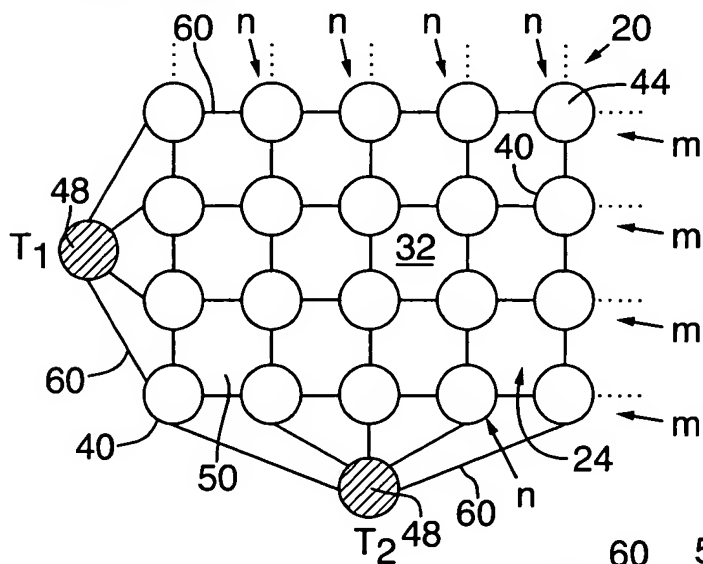


FIG. 3b

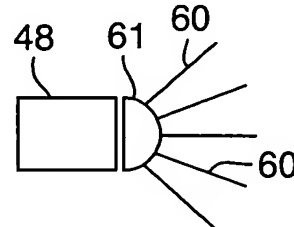


FIG. 4

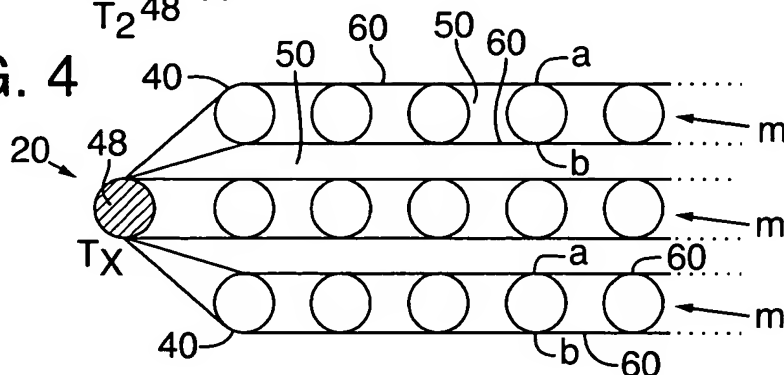


FIG. 5

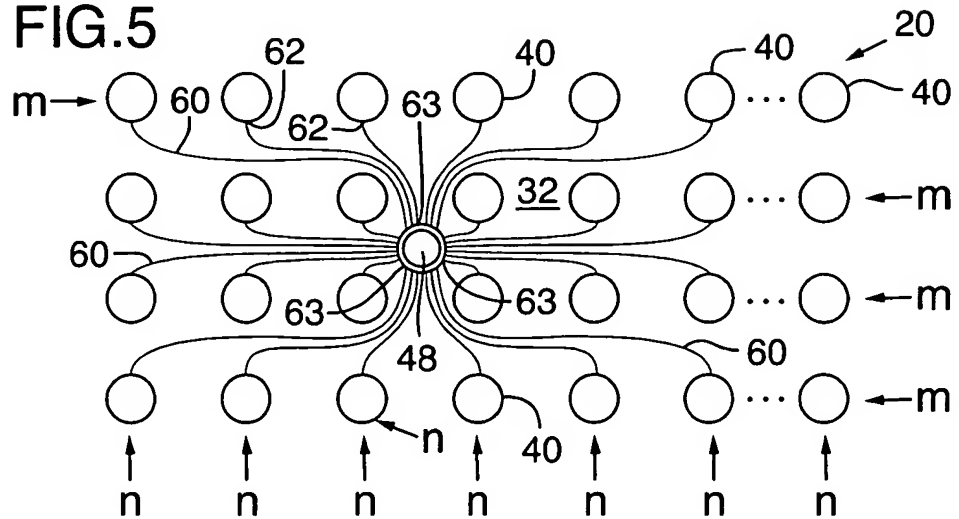


FIG. 6

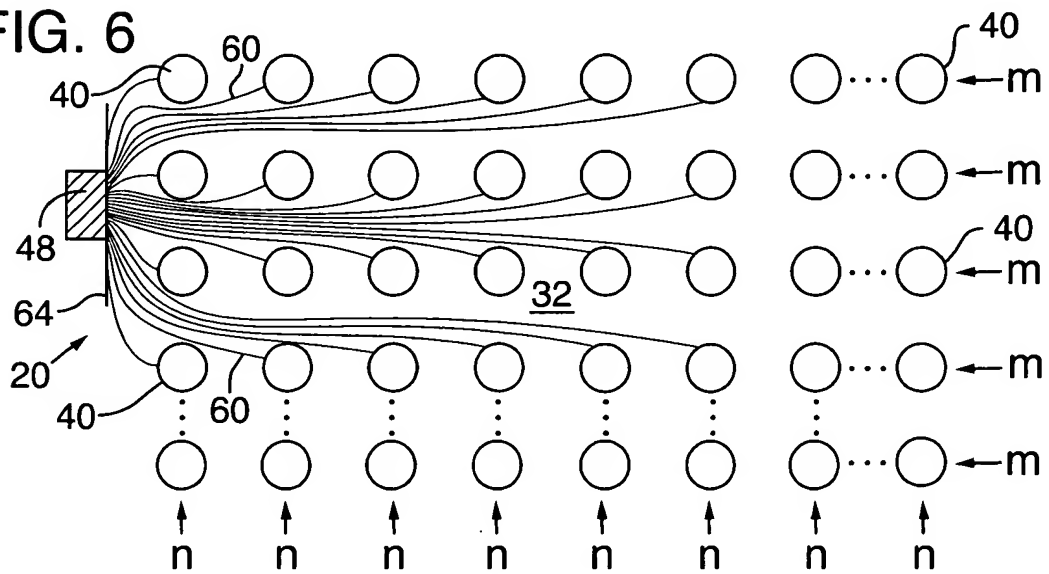


FIG. 7

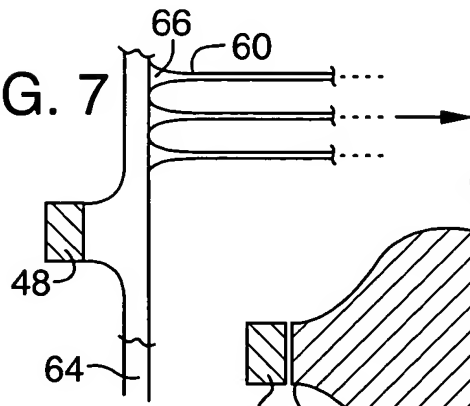


FIG. 8

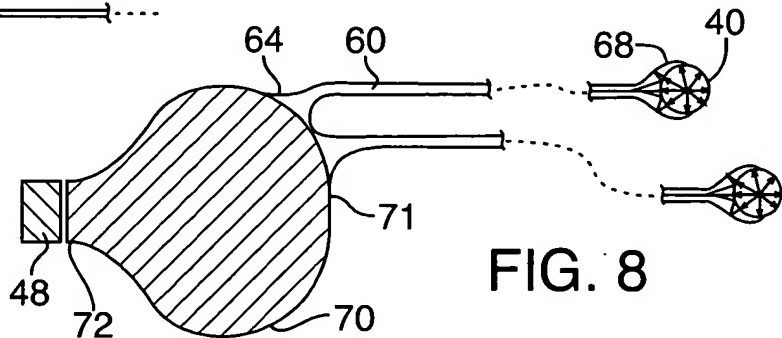


FIG. 9

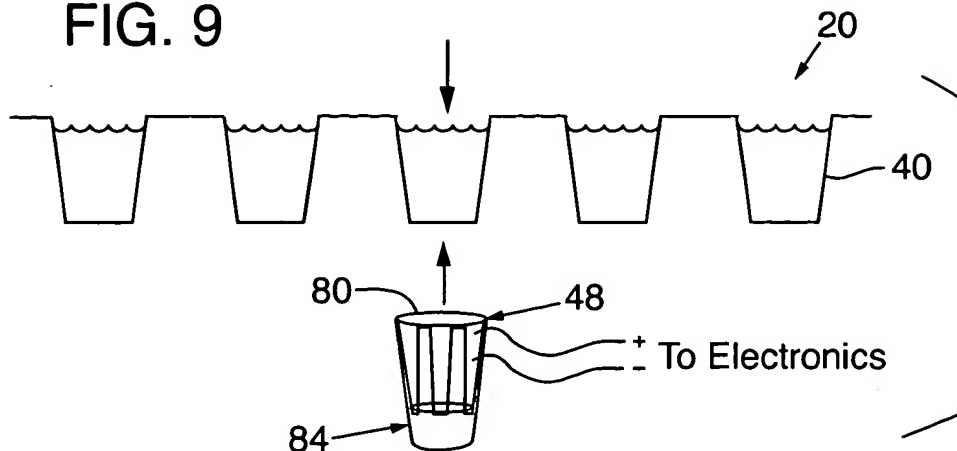


FIG. 10

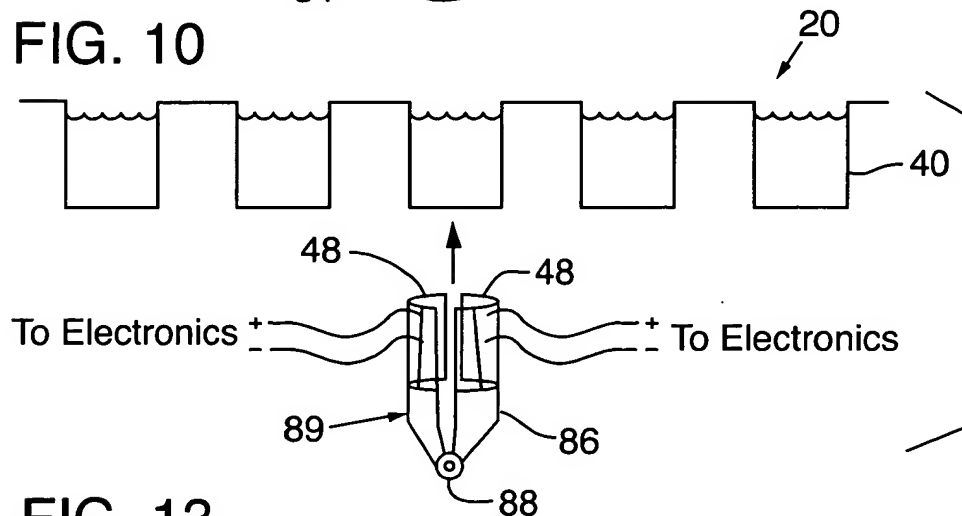
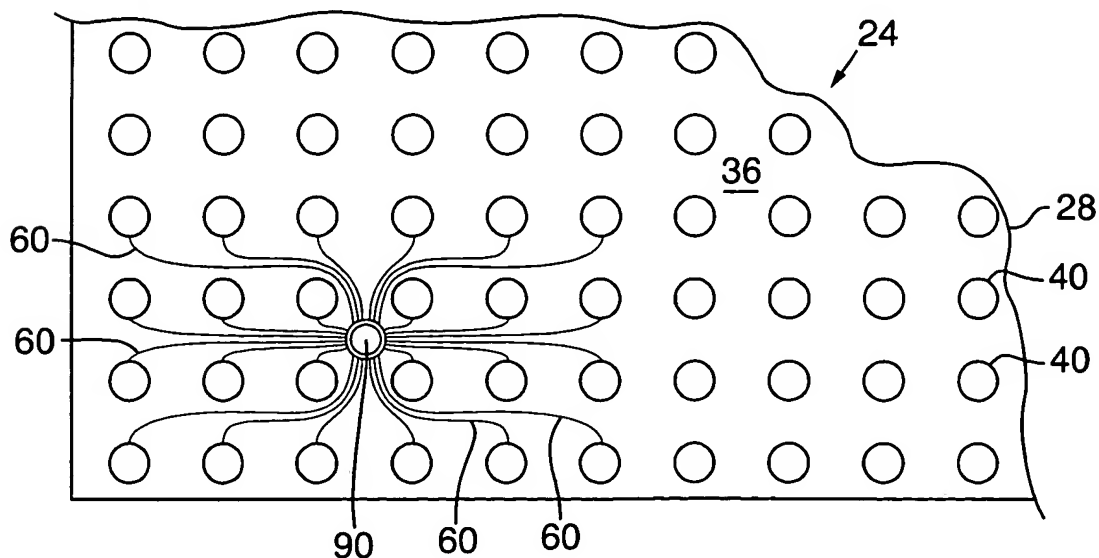


FIG. 13



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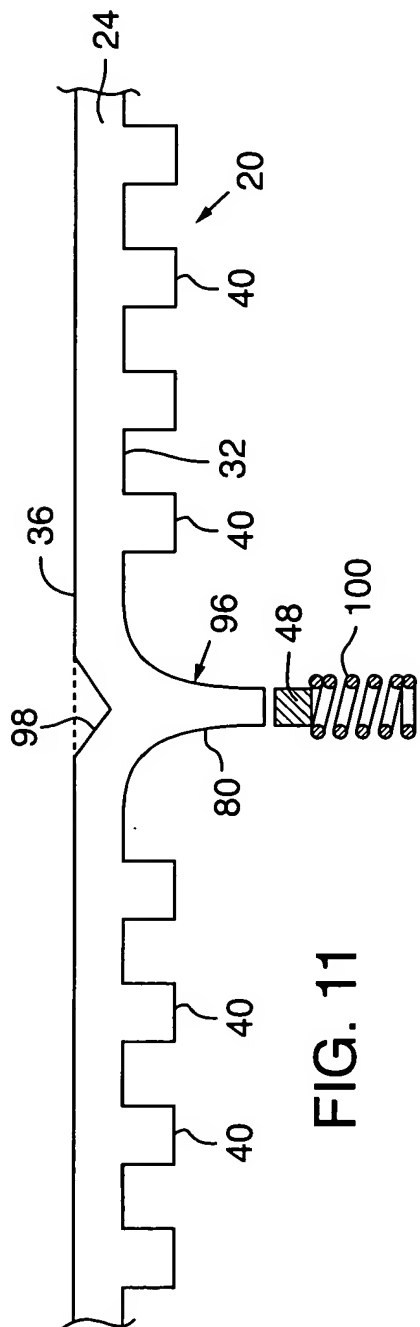


FIG. 11

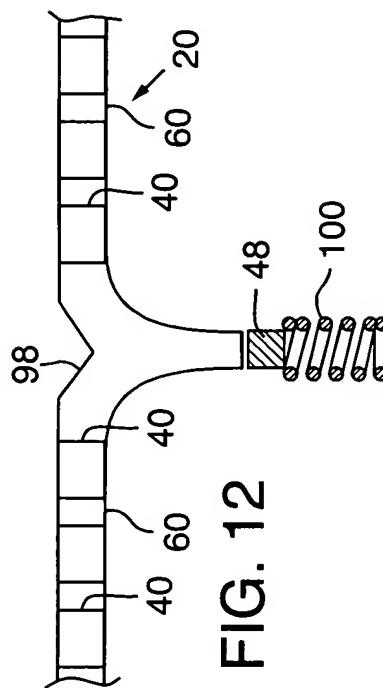


FIG. 12

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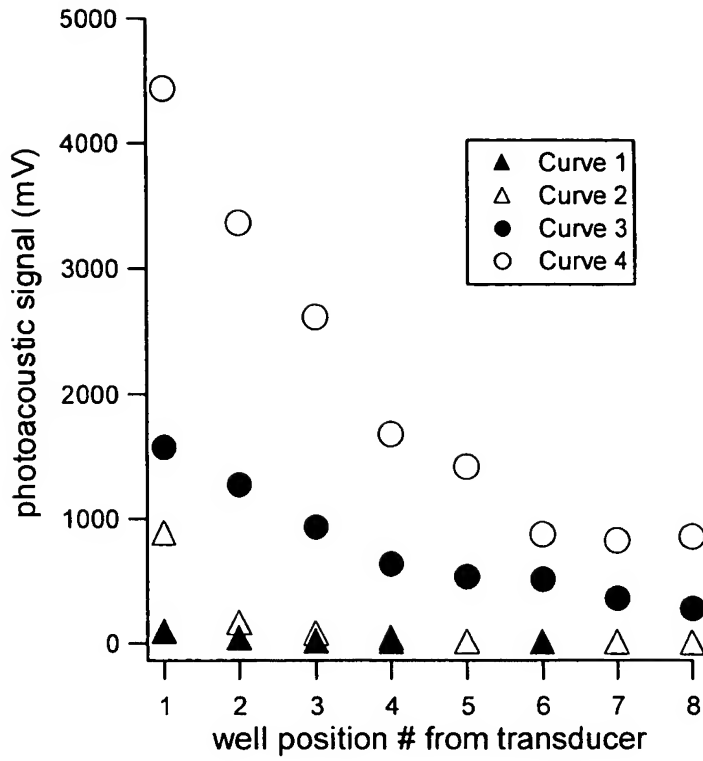


FIG. 14

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FIG. 15a

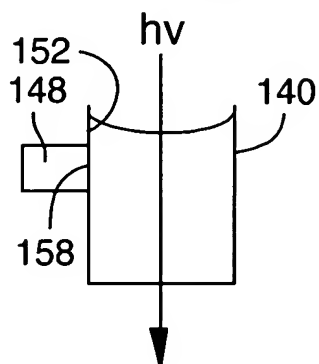


FIG. 15b

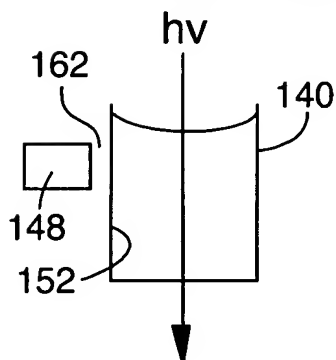
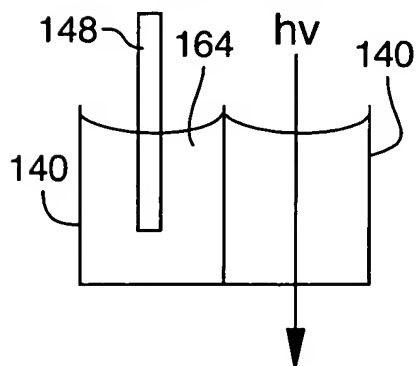


FIG. 15c



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A cross-sectional view of a semiconductor device. The device consists of a substrate 142 with a layer 148 on top. A patterned layer 136 is formed on layer 148. A top layer 120 is formed on layer 136, with openings 140. A side layer 128 is formed on the left side of the top layer 120. A contact layer 138 is formed on the right side of the top layer 120.

